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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,316	11/20/2003	Motohiko Bungo	P03-1004	3093

56026 7590 12/14/2005

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EXAMINER	
NAMAZI, MEHDI	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,316	BUNGO ET AL.	
	Examiner	Art Unit	
	Mehdi Namazi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 6-9* is/are rejected.

7)☐ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application filed November 20, 2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1- 3, and 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakata et al. (US. No. 6,788,592).

As per claims 1, 7, 8, and 9, Nakata teaches memory module standardized and connectable to a computer body generating a predetermined number of address signals and a plurality of select signals representing a select or unselected state of each of memory spaces having a capacity corresponding to the predetermined of the address signals (fig. 3; col. 2, lines 18-20, with predetermined addresses of A0-A21, and signal selects CS1, CS2, to control memory capacity) the memory module comprising: a

memory receiving a memory select signal representing a select or unselected state and a plurality of address signals greater than the predetermined number of the address signals, and permitting data corresponding the plurality of the address signals to be accessible when the memory select signal represents a selected state (col. 4, lines 44-64; fig. 5, shows the using CS1 or CS2 and additional address signal A22 for controlling the higher and lower space of memory) ; and a memory circuit receiving the predetermined number of the address signals and a plurality of select signals from the computer body (fig. 5, element 16, shows the connection between memory circuit and the processor 10), generating the memory select signal and an additional address signal added to the predetermined number of the address according to the inputted select signals, and providing the generated memory select signal, the generated additional address signal, and the predetermined number of the inputted address signals to the memory to permit the computer body to access data corresponding thereto(cols 5-6, lines 63-13; fig. 6, element 16 shows a memory which is using CS1 to generate additional address signal A22 in order to increase the memory space).

As per claim 2, Nakata teaches the memory circuit makes the memory select signal represent a selected state of the memory when either of the plurality of the inputted select signals represents a selected state of the memory space, and makes the memory select signal represent an unselected state of the memory when all the plurality of the inputted select signals represent an unselected state of the memory space (fig. 6, shows different mode of using CS1 and CS2, wherein by using CS2 with A0-A20 (memory B), and CS1 for A0-A22 (memory A) for different capacity of Memory).

As per claim 3, Nakata teaches the computer body generates two types of select signals representing a selected or unselected state of two memory spaces of a capacity corresponding to the predetermined number of the address signals, and wherein the memory circuit receives either of the two types of the select signals from the computer body, and provides the either of the select signals as the additional address to the memory (col. 4, lines 25-43).

As per claim 6, Nakata teaches the additional address signal represents an address upper than one represented by the predetermined number of the address signals (fig. 8, element 28).

Allowable Subject Matter

3. Claims 4, and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 571-272-4209. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mehdi Namazi
December 11, 2005

12/12/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER